Claims

[c1] 1.A driver circuit comprising:

a logical enable device having an input and an output;

a driving transistor having a gate connected to said output of said logical enable device; and at least one of:

a pull-down booster circuit connected to said gate of said driving transistor, wherein said pull-down booster circuit is adapted to dynamically pull-down a voltage at said gate of said driving transistor when a voltage level at said input to said logical enable device changes from a first voltage to a second voltage; and

a pull-up booster circuit connected said gate of said driving transistor, wherein said pull-up booster circuit is adapted to dynamically pull-up a voltage at said gate of said driving transistor when a voltage level at said input to said logical enable device changes from said second voltage to said first voltage.

[c2] The driver circuit in claim 1, wherein said pull-down booster circuit comprises:

a logical NAND device having first and second inputs, wherein said first input is connected to an input signal supplied to said logical enable device; and

a pull-down transistor having a gate connected to an output of said NAND device, a source connected to said gate of said driving transistor, and a drain connected to ground.

[c3] The driver circuit in claim 2, wherein said second input of said logical NAND device is connected to said gate of said driving transistor, such

that said logical NAND device dynamically activates said pull-down transistor to pull-down said gate of said driving transistor to ground only while said input signal is at said second voltage level and said gate of said driving transistor is also at said second voltage level.

[c4] The driver circuit in claim 2, further comprising at least one pull-down delay element between said logical NAND device and said pull-down transistor.

[c5] The driver circuit in claim 4, wherein said pull-down delay element is connected in parallel with a signal line running between said logical NAND device and said pull-down transistor such that a delay created by said pull-down delay element is dynamically varied depending a difference between a voltage level of said input signal supplied to said logical enable device and a voltage level at said gate of said driving transistor.

[c6] The driver circuit in claim 2, wherein said transistor comprises a P-type transistor directly connected to said logical NAND device.

[c7] The driver circuit in claim 2, wherein said transistor comprises an N-type transistor and said circuit further comprises an inverter positioned between said logical NAND device and said transistor.

[c8] The driver circuit in claim 1, wherein said pull-up booster circuit comprises:

a logical NOR device having first and second inputs, wherein said first input is connected to an input signal supplied to said logical enable

device; and

a pull-up transistor having a gate connected to an output of said NOR device, a drain connected to said gate of said driving transistor, and a source connected to a first voltage level.

[c9] The driver circuit in claim 8, wherein said second input of said logical NOR device is connected to said gate of said driving transistor, such that said logical NOR device activates said pull-up transistor to pull-up said gate of said driving transistor to said first voltage level only while said input signal supplied to said logical enable device is at said first voltage level and said gate of said driving transistor is also at said first voltage level.

[c10] The driver circuit in claim 8, further comprising at least one pull-down delay element between said logical NOR device and said pull-down transistor.

[c11] The driver circuit in claim 10, wherein said pull-down delay element is connected in parallel with a signal line running between said logical NOR device and said pull-down transistor such that a delay created by said pull-down delay element is dynamically varied depending upon a difference between a voltage level of said input signal supplied to said logical enable device and a voltage level at said gate of said driving transistor.

[c12] The driver circuit in claim 8, wherein said transistor comprises an N-type transistor directly connected to said logical NOR device.

[c13] The driver circuit in claim 8, wherein said transistor comprises a P-type transistor and said circuit further comprises an inverter positioned between said logical NOR device and said transistor.

[c14] A driver circuit comprising:

a logical enable device;

a driving transistor having a gate connected to an output of said logical enable device; and

a pull-down booster circuit comprising:

a logical NAND device having first and second inputs, wherein said first input is connected to an input signal supplied to said logical enable device; and

a pull-down transistor having a gate connected to an output of said NAND device, a source connected to said gate of said driving transistor, and a drain connected to ground,

wherein said second input of said logical NAND device is connected to said gate of said driving transistor, such that said logical NAND device dynamically activates said pull-down transistor to pull-down said gate of said driving transistor to ground only while said input signal and said gate of said driving transistor are at the same logic level.

[c15] The driver circuit in claim 14, further comprising at least one pull-down delay element between said logical NAND device and said pull-down transistor.

[c16] The driver circuit in claim 15, wherein said pull-down delay element is connected in parallel with a signal line running between said logical

NAND device and said pull-down transistor such that a delay created by said pull-down delay element is dynamically varied depending a difference between a voltage level of said input signal supplied to said logical enable device and a voltage level at said gate of said driving transistor.

[c17] The driver circuit in claim 14, wherein said pull-down transistor comprises a P-type transistor directly connected to said logical NAND device.

[c18] The driver circuit in claim 14, wherein said pull-down transistor comprises an N-type transistor and said circuit further comprises an inverter positioned between said logical NAND device and said transistor.

[c19] A driver circuit comprising:

a logical enable device;

a driving transistor having a gate connected to an output of said logical enable device; and

a pull-up booster circuit comprising:

a logical NOR device having first and second inputs, wherein said first input is connected to an input signal supplied to said logical enable device; and

a pull-up transistor having a gate connected to an output of said NOR device, a drain connected to said gate of said driving transistor, and a source connected to a first voltage level,

wherein said second input of said logical NOR device is connected to

said gate of said driving transistor, such that said logical NOR device activates said pull-up transistor to pull-up said gate of said driving transistor to said first voltage level only while said input signal supplied to said logical enable and said gate of said driving transistor are at the same logic level.

[c20] The driver circuit in claim 19, further comprising at least one pull-down delay element between said logical NOR device and said pull-down transistor.

[c21] The driver circuit in claim 20, wherein said pull-down delay element is connected in parallel with a signal line running between said logical NOR device and said pull-down transistor such that a delay created by said pull-down delay element is dynamically varied depending a difference between a voltage level of said input signal supplied to said logical enable device and a voltage level at said gate of said driving transistor.

[c22] The driver circuit in claim 19, wherein said pull-down transistor comprises an N-type transistor directly connected to said logical NOR device.

[c23] The driver circuit in claim 19, wherein said pull-down transistor comprises a P-type transistor and said circuit further comprises an inverter positioned between said logical NOR device and said transistor.

[c24] A driver circuit comprising:
a logical enable device;
a pull-down booster circuit comprising:

a logical NAND device having first and second inputs, wherein said first input is connected to an input signal supplied to said logical enable device; and

a pull-down transistor having a gate connected to an output of said NAND device, a source connected to said gate of said driving transistor, and a drain connected to ground,

wherein said second input of said logical NAND device is connected to said gate of said driving transistor, such that said logical NAND device dynamically activates said pull-down transistor to pull-down said gate of said driving transistor to ground only while said input signal and said gate of said driving transistor are both at a first logic level; and

a pull-up booster circuit comprising:

a logical NOR device having first and second inputs, wherein said first input is connected to an input signal supplied to said logical enable device; and

a pull-up transistor having a gate connected to an output of said NOR device, a drain connected to said gate of said driving transistor, and a source connected to a first voltage level,

wherein said second input of said logical NOR device is connected to said gate of said driving transistor, such that said logical NOR device activates said pull-up transistor to pull-up said gate of said driving transistor to said first voltage level only while said input signal supplied to said logical enable and said gate of said driving transistor are both at a second logic level.

[c25] The driver circuit in claim 24, further comprising at least one pull-down delay element between said logical NAND device and said pull-down

transistor and at least one pull-up delay element between said logical NOR device and said pull-up transistor.

[c26] The driver circuit in claim 25, wherein said pull-down delay element is connected in parallel with a signal line running between said logical NAND device and said pull-down transistor and said pull-up delay element is connected in parallel with a signal line running between said logical NOR device and said pull-up transistor, such that delays created by said pull-down delay element and said pull-up delay element are dynamically varied depending a difference between a voltage level of said input signal supplied to said logical enable device and a voltage level at said gate of said driving transistor.

[c27] The driver circuit in claim 24, wherein said pull-down transistor comprises a P-type transistor directly connected to said logical NAND device and said pull-up transistor comprises a N-type transistor directly connected to said logical NOR device.

[c28] The driver circuit in claim 24, wherein said pull-down transistor comprises an N-type transistor and said circuit further comprises an inverter positioned between said logical NAND device and said pull-up transistor and wherein said pull-up transistor comprises a P-type transistor and said circuit further comprises and inverter positioned between said logical NOR device and said pull-up transistor.

[c29] A pull-down booster circuit for use with a driver having a logical enable device, said pull-down booster circuit comprising:
a logical NAND device having first and second inputs, wherein said first

input is connected to an input signal supplied to said logical enable device; and

a transistor having a gate connected to an output of said NAND device, a source connected to an output of said logical enable device, and a drain connected to ground,

wherein said second input of said logical NAND device is connected to said output of said logical enable device, such that said logical NAND device dynamically activates said transistor to pull-down said output of said logical enable device to ground only while said input signal and a signal on said output of said logical enable device are at the same logic level.

[c30] The pull-down booster circuit in claim 29, further comprising at least one pull-down delay element between said logical NAND device and said transistor.

[c31] The pull-down booster circuit in claim 30, wherein said pull-down delay element is connected in parallel with a signal line running between said logical NAND device and said transistor such that a delay created by said pull-down delay element is dynamically varied depending upon a difference between a voltage level of said input the signal supplied to said logical enable device and a voltage level at said output of said logical enable device.

[c32] The pull-down booster circuit in claim 29, wherein said transistor comprises a P-type transistor directly connected to said logical NAND device.

[c33] The pull-down booster circuit in claim 29, wherein said transistor comprises an N-type transistor and said circuit further comprises an inverter positioned between said logical NAND device and said transistor.

[c34] A pull-up booster circuit for use with a driver having a logical enable device, said pull-up booster circuit comprising:
a logical NOR device having first and second inputs, wherein said first input is connected to an input signal supplied to said logical enable device; and
a transistor having a gate connected to an output of said NOR device, a drain connected to an output of said logical enable device, and a source connected to a first voltage level,
wherein said second input of said logical NOR device is connected to said output of said logical enable device, such that said logical NOR device activates said transistor to pull-up said output of said logical enable device to said first voltage level only while said input signal supplied to said logical enable device and a signal on said output of said logical enable device at are at the same logic level.

[c35] The pull-up booster circuit in claim 34, further comprising at least one pull-down delay element between said logical NOR device and said transistor.

[c36] The pull-up booster circuit in claim 35, wherein said pull-down delay element is connected in parallel with a signal line running between said logical NOR device and said transistor such that a delay created by said

pull-down delay element is dynamically varied depending upon a difference between a voltage level of said input the signal supplied to said logical enable device and a voltage level at said output of said logical enable device.

[c37] The pull-up booster circuit in claim 34, wherein said transistor comprises an N-type transistor directly connected to said logical NOR device.

[c38] The pull-up booster circuit in claim 34, wherein said transistor comprises a P-type transistor and said circuit further comprises an inverter positioned between said logical NOR device and said transistor.